### Session Timetable

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<td>10:00-10:30</td>
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**NS1**: Security and Fault Simulation  
**NS2**: New Technologies  
**NS3**: Online Testing  
**NS4**: Test  
**NS5**: Design  
**NS6**: Analog & FPGA

**SS1**: Emerging Resistive Memories Technologies  
**SS2**: Bio-electronic Interfaces  
**SS3**: Hardware Security and Trust  
**SS4**: Modelization of laser-based attacks for design-time security analysis  
**SS5**: Recent Advances in SAT-based ATPG  
**SS6**: Design and Test Methods for Emerging Technologies
DTIS 2014 Foreword

On behalf of the Steering, Organizing and Program Committees, we would like to welcome you to the International Conference on Design and Technology of Integrated systems in nanoscale era (DTIS) 2014, an event devoted to presenting and discussing scientific trends, emerging results, hot topics, and practical applications in the area of design and technology of integrated systems.

DTIS 2014 is the 9th edition of this conference and is held in Santorini island, Greece. Santorini is essentially what remains after an enormous volcanic explosion that destroyed the earliest settlements on a formerly single island, and created the current geological caldera. The capital, Fira, clings to the top of the cliff looking down on the lagoon. The island is the site of one of the largest volcanic eruptions in recorded history: the Minoan eruption (sometimes called the Thera eruption), which occurred some 3600 years ago at the height of the Minoan civilization. The eruption may have led to the collapse of the Minoan civilization on the island of Crete, 110 km to the south, through a gigantic tsunami. Another popular theory holds that the Thera eruption is the source of the legend of Atlantis.

DTIS 2014 starts on Tuesday, May 6th, implements a three-day technical program, together with an attractive social event, and ends on Thursday, May 8th. The conference technical program consists of three keynote addresses, scientific paper presentations, special sessions and two poster sessions. DTIS received a large number of contributions from all over the world. An electronic version of the formal proceedings has been included in a flash memory that will be distributed to conference attendees.

DTIS2014 is the achievement of the contributions by many volunteers, who give generously their time to contribute to the success of the symposium. We would like to thank all of them for their efforts.

We are confident that you will find DTIS2014 a productive and exciting experience, and would like to welcome you in Santorini.

Ioannis Voyiatzis
DTIS 2014 General Chair

Paolo Prinetto
DTIS 2014 Program Chair

M. Renovell & M. Masmoudi
DTIS 2014 General Vice-Chairs

Giorgio Di Natale
DTIS 2014 Program Vice-Chair
08:30 - 08:45  Registration
08:45 – 09:00  Opening Session
09:00 – 10:00  Keynote #1
Towards Resilient Cyber-Physical Systems: The ADREAM Project
Jean ARLAT (LAAS-CNRS - France)
Chair: Michel Renovell, LIRMM - France

10:00 – 11:00  Coffee Break & Poster Session #1
New Floating Inductance Simulator Employing a Single ZC-VDTA and One Grounded Capacitor
Arda GUNEY¹, Hakan KUNTMAN² (¹Yildiz Technical University – Turkey, ²Istanbul Technical University - Turkey)
Easily Verified IP Watermarking
Haridimos VERGOS, Anastasios BIKOS (University of Patras - Greece)
On the Design of Efficient Modulo 2ⁿ⁺¹ Multiply-Add-Add Units
Costas EFSTATHIOU¹, Kostas TSOUMANIS², Kiamal PEKMESTZI², Ioannis VOYIATZIS² (¹TEI of Athens – Greece, ²National Technical University of Athens – Greece)
Low Overhead Output Response Compaction in RAS Architectures
Ioannis VOYIATZIS, Costas EFSTATHIOU, Cleo SGOUROPOULOU (TEI of Athens – Greece)

11:00 – 12:30  Special Session on Emerging Resistive Memories Technologies: Opportunities and Challenges
Organized by Said Hamdioui (Delft University of Technology - Netherlands)
Technology, Modelling and Design Constraints
Hassen Aziza (Aix Marseille University - France)
Alternative Topologies for Memristor Based Crossbar Memories
Georgios, Sirakoulis (Democritus University of Thrace - Greece)
Testability and Design for Test for Memristor Based Memories
Said Hamdioui (Delft University of Technology - the Netherlands)

11:00 – 12:30  Security and Fault Simulation
Chair: Giorgio Di Natale, LIRMM - France
Hardware Implementation of Montgomery Multiplication for Embedded Cryptosystems
Mohamed ISSAD¹, Bachir BOUDRAA² (¹Centre de Développement des Technologies Avancées – Algeria, ²Université des Sciences et de la Technologie Houari Boumediene - Algeria)
Electromagnetic Injection Attacks on Embedded Devices: a Model of Probe-Circuit Power Coupling
Diego ALBERTO, Paolo MAISTRI, Regis LEVEUGLE (TIMA Laboratory - France)
A Survey on Simulation-based Fault Injection Tools for Complex Systems
Giorgio DI NATALE, Maha KOOLI (LIRMM - France)

12:30 – 14:00 Lunch

14:00 – 15:30 New Technologies
Chair: Arda Guney, Yildiz Technical University – Turkey

An Electrostatically Doped Planar Device Concept
Tillmann KRAUSS¹, Frank WESSELY², Udo SCHWALKE²
(¹Technische Universität Darmstadt – Germany, ²TU Darmstadt – Germany)

2nd Generation Bilayer Graphene Transistors for Applications in Nanoelectronics
Pia Juliane WESSELY¹, Udo SCHWALKE²
(¹Technische Universität Darmstadt – Germany, ²TU Darmstadt - Germany)

Dependence of Annealing Temperature on Cluster Formation During in Situ Growth of CNTs
Martin KEYN¹, Andreas KRAMER¹, Udo SCHWALKE²
(¹Technische Universität Darmstadt – Germany, ²TU Darmstadt - Germany)

15:30 – 16:00 Coffee Break

16:00 – 17:30 Special Sessions on Bio-electronic Interfaces
Organized by Fabien SOULIER (LIRMM - France)
Chair: Gildas Leger, IMSE-CNM - Spain

Bio-electronic interaction: principle and applications
Noelle LEWIS (University of Bordeaux, IMS – France)

Bio-impedance spectroscopy: Problems to avoid
Eric MCADAMS (INS-A CNRS, Lyon – France)

MicroElectrode Array (MEA), a way to access to the Neural code for in-vitro and in-vivo applications, principle and fabrication.
Lionel ROUSSEAU, Gaëlle LISSORGUES (ESIEE Paris – France)

16:00 – 17:30 Online Testing
Chair: Lorena Anghel, TIMA - France

Linking Aging Measurements of Health-Monitors and Specifications for Multi-Processor SoCs
Hans KERKHOFF, Jinbo WAN, Yong ZHAO
(University of Twente – Netherlands)

Accurate Multiplexed Test Structure for Transistor Threshold Voltage Difference Extraction
Loic WELTER¹, Philippe DREUX¹, Jean Michel PORTAL², Hassen AZIZA²
(¹STMicroelectronics – France, ²IM2NP – France)

Accumulator-based Self-Adjusting Output Data Compression for Embedded Word-Organized DRAMs
Ioannis VOYIATZIS, Costas EFSTATHIOU, Cleo SGOUROPOULOU
(TEI of Athens - Greece)
Wednesday May 7

09:00 – 10:00  **Keynote #2**  
*Addressing Trends & Challenges in Emerging Technology Nodes*  
Yervant ZORIAN (Synopsys Inc – USA)  
Chair: Giorgio Di Natale, LIRMM - France

10:00 – 11:00  **Coffee Break & Poster Session #2**  
*A Web EDA Tool for the Automatic Generation of Synthesizable VHDL Architectures for a Rapid Design Space Exploration*  
Minas DASYGENIS (University of Western Macedonia - Greece)

*Radio Network Optimisation Using Simulated Annealing*  
Khrouf Mohmed BECHIR, Maaloul HENDA  
(Telecom, Service & Computer Science Engineering - Tunisia)

*Slack Removal for Enhanced Reliability and Trust*  
Samah SAEED¹, Abishek RAMDAS², Ozgur SINANOGLU³  
(¹Polytechnic Institute of New York University - USA, ²Qualcomm, San Diego, CA - USA, ³NYU-Abu Dhabi - United Arab Emirates)

11:00 – 12:30  **Special Session on Hardware Security and Trust**  
Organized by Ozgur SINANOGLU  
(NYU-Abu Dhabi - United Arab Emirates)

Chair: Ioannis Voyiatzis, TEI of Athens - Greece

*Design-for-Trust Techniques*  
Ozgur SINANOGLU (NYU-Abu Dhabi – United Arab Emirates)

*Delay Constraint Enumeration Assisted Modeling of Arbiter PUF*  
Hitesh KAPOOR, Rajat Subhra CHAKRABORTY, and Debdeep MUKHOPADHYAY  
(Indian Institute of Technology – India)

*Investigating Large Integer Arithmetic on Intel Xeon Phi SIMD Extensions*  
Anastasis KELIRIS, Michail MANIATAKOS  
(NYU-Abu Dhabi – United Arab Emirates)

11:00 – 12:30  **Test**  
Chair: Ioana Vatajelu, Politecnico di Torino, Italy

*ATPG for Transition Faults of Pipelined Threshold Logic Circuits*  
Ashok Kumar PALANISWAMY, Spyros TRAGoudas, Themistoklis HANIOTAKIS (Southern Illinois University Carbondale - USA)

*Stuck-at Fault Diagnosis in Scan Chains*  
Helen-Maria DOUNAVI, Yiorgos TSIATOUHAS  
(University of Ioannina - Greece)

12:30 – 14:00  **Lunch**
14:00 – 15:30  
**Special Session on Modelization of laser-based attacks for design-time security analysis of integrated systems**

Organized by Regis LEVEUGLE (TIMA Laboratory - France)

Chair: Costas Efstathiou, TEI of Athens, Greece

**Brief introduction to the context**

Regis LEVEUGLE (TIMA Laboratory - France)

**Laser attacks on integrated circuits: from CMOS to FDSOI**

Jean-Max DUTERTRE, Stephan DE CASTRO, Alexandre SARAFIANOS, Noemie BOHER, Bruno ROUZEYRE, Mathieu Lisart, Joel DAMIENS, Philippe CANDELIERS, Marie-Lise FLOTTES and Giorgio DI NATALE

(1ENSM.SE – France, 2STMicroelectronics, Rousset – France, 3STMicroelectronics, Crolles – France, 4LIRMM – France)

**Layout-Aware Laser Fault Injection Simulation and Modeling: from physical level to gate level**

Feng LU, Giorgio DI NATALE, Marie-Lise FLOTTES, Bruno ROUZEYRE, Guillaume HUBERT

(1LIRMM – France, 2ONERA – France)

**On error models for RTL security evaluations**

Pierre VANHAUWAERT, Paolo MAISTRI, Regis LEVEUGLE, Athanasios PAPADIMITRIOU, David HELY, Vincent BEROULLE

(1TIMA – France, 2Univ. Grenoble Alpes – France)

14:00 – 15:30  
**Design**

Chair: Maha Kooli, LIRMM - France

**Generation and Validation of Multioperand Carry Save Adders from the Web**

Minas DASYGENIS (University of Western Macedonia - Greece)

**Evaluation of Image Deblurring Algorithms for Real-Time Applications**

Marco INDACO, Daniele ROLFO, Pascal TROTTA, Airo Farulla GIUSEPPE, Russo LUDOVICO (Politecnico di Torino - Italy)

**An Inter-Processor Communication Interface for Data-Flow Centric Heterogeneous Embedded Multiprocessor Systems**

Luca CASSANO, Dario COZZI, Dirk JUNGEWELTER, Sebastian KORF, Jens HAGEMEYER, Mario PORRMANN, Cinzia BERNARDESCHI

(1University of Pisa – Italy, 2Politecnico di Milano – Italy, 3Bielefeld University - Germany)

15:30 – 17:30  
**Social Event**
Thursday May 8

**Registration**

**09:00 – 10:00**  
**Keynote #3**  
*System Physician on Chip (SPOC): Dynamic Adaptation for Resilient Integrated Circuits and Systems*  
Krish Chakrabarty (Duke University – USA)  
Chair: Paolo Prinetto, Politecnico di Torino, Italy

**10:00 – 10:30**  
**Coffee Break**

**10:30 – 12:30**  
**Analog and FPGA**  
Chair: Michel Renovell, LIRMM, France

*Low Voltage Analog Readout Channel based on Gain-Boosted Amplifiers*  
Juan GOMEZ-GALAN, Rafael LOPEZ-AHUMADA, Trinidad SANCHEZ-RODRIGUEZ, Manuel SANCHEZ-RAYA, Manuel PEDRO, Raul JIMENEZ (University of Huelva - Spain)

*Power Consumption Analysis for Mesh based FPGA*  
Sonda CHTOUROU¹, Zied MARRAKCHI², Mohamed ABID¹, Habib MEHREZ³  
(¹University of Sfax – Tunisia, ²Flexras Technologies Industrial Society – France, ³University of Pierre and Marie Curie - France)

*Doubly-Segmented Current-Steering DAC Calibration*  
Gildas LEGER (IMSE-CNM - Spain)

*Exploration and Optimization of Heterogeneous Interconnect Fabric of 3D Tree-based FPGA*  
Zied MARRAKCHI, Vinod PANGRACIOUS, Habib MEHREZ  
(University of Pierre and Marie Curie – France)

**12:30 – 14:00**  
**Lunch**

**14:00 – 15:30**  
**Special Sessions on Recent Advances in SAT-based ATPG: Non-Standard Fault Models, Multi Constraints and Optimization**  
Organized by Bernd BECKER¹, Rolf DRECHSLER²  
(¹University of Freiburg – Germany, ²University of Bremen - Germany)

Chair: Bernd Becker, University of Freiburg – Germany
14:00 – 15:30  **Special Session on Design and Test Methods for Emerging Technologies**

Organized by Aida TODRI-SANIAL¹, Theocharis THEOCHARIDES², Maria MICHAEL²

¹LIRMM-CNRS - France, ²University of Cyprus - Cyprus

Chair: Ioannis Voyiatzis, TEI of Athens, Greece

**Recent Advances in Single- and Multi-Site Test Optimization for DVS-based SoCs**

Chrysovalantis KAVOUSIANOS¹, Krishnendu CHAKRABARTY²

¹University of Ioannina – Greece, ²Duke University – USA

**Physical Design and Testing of Nano Magnetic Architectures**

Giovanna TURVANI, Matteo BOLLO, Riente FABRIZIO, Marco VACCA, Mariagrazia GRAZIANO, Maurizio ZAMBONI

(Politecnico di Torino – Italy)

**3D/ 2.5D Stacked IC Cost Modeling and Test Flow Selection**

Said HAMDIOUI (Delft University of Technology – Netherlands)

**Design and Test Methods for Emerging Technologies**

Mehdi TAHOORI (Karlsruhe Institute of Technology – Germany)

15:30 – 16:00  **Closing Session**

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**DTIS 2014 Committees**

*General Chair:* Ioannis Voyiatzis - TEI of Athens, Greece

*General Vice-Chairs:* Michel Renovell - LIRMM, France  Mohamed Masmoudi - ENIS, Tunisia

*Program Chair:* Paolo Prinetto - Politecnico di Torino, Italy

*Program Vice-Chair:* Giorgio Di Natale - LIRMM, France

*Special Session Chair:* Elena Ioana Vatajelu - Politecnico di Torino, Italy

*Publication Chair:* Alberto Bosio - LIRMM, France

*Publicity Chair:* Marco Indaco - Politecnico di Torino, Italy

*Steering Committee:*

Michel Renovell, LIRMM, France

Mohamed Masmoudi, ENIS, Tunisia

Said Hamdioui, TUdelft, The Netherlands

Patrick Girard, LIRMM, France

Ioannis Voyiatzis, TEI, Greece